Claims

[c1] Unknown;me;ClaireKo;What is claimed is:

1.A structure of an embedded channel write/erase flash memory cell, comprising mainly:

an N-substrate;

a flash memory cell region comprising mainly: and

a deep P-well formed on in said substrate;

an N-well formed on in said deep P-well, a deep P-type region and a shallow p-type region being implanted in predetermined positions of said N-well;and

a stacked gate formed on said N-well;

a CMOS device region comprising mainly:

a first deep P-well formed on in said substrate;

a first N-well formed on in said first deep P-well, a plurality of p-type regions being implanted in predetermined positions of said first N-well;

a second deep P-well formed on in said substrate; and

a second N-well formed on in said second deep P-well, a plurality of p-type regions being implanted in predetermined positions of said second N-well.

[c2] 2.The structure of an embedded channel write/erase flash memory cell as claimed in claim 1, wherein an oxide layer is further provided between said N-well and said stacked gate of said flash memory cell region.

[c3] 3.The structure of an embedded channel write/erase flash memory cell as claimed in claim 2, wherein a smiling effect pattern is caused by oxidation between said stacked gate and said oxide layer.

[c4] 4.The structure of an embedded channel write/erase flash memory cell as claimed in claim 1, wherein an n-type region is further implanted in said deep p-type region in said N-well of said flash memory cell region to be used as a drain.

[c5] 5.The structure of an embedded channel write/erase flash memory cell as claimed in claim 1, wherein the implanted depth of said deep p-type region in said N-well of said flash memory cell region is larger than that of said shallow p-type region.

[c6] 6.The structure of an embedded channel write/erase flash memory cell as claimed in claim 1, wherein said deep p-type region in said N-well of said flash memory cell region is connected with one end of said shallow p-type region.

[c7] 7.The structure of an embedded channel write/erase flash memory cell as claimed in claim 1, wherein an n-type region is further implanted at the other side of said shallow p-type region in said N-well of said flash memory cell region to be used as a source.

[c8] 8.The structure of an embedded channel write/erase flash memory cell as claimed in claim 7, wherein a field oxide layer and an n-type ion channel barrier layer can also be provided between said n-type region and said shallow p-type region in said N-well, said n-type ion channel barrier layer being disposed below said field oxide layer.

[c9] 9.The structure of an embedded channel write/erase flash memory cell as claimed in claim 14, wherein said n-type region implanted in said deep p-type region of said flash memory cell region is connected to said deep p-type region via an electrical short circuit.

[c10] 10.The structure of an embedded channel write/erase flash memory cell as claimed in claim 9, wherein said electrical short circuit is formed by using a metal contact to penetrate a junction of said n-type region in said deep p-type region and said deep p-type region.

[c11] 11.The structure of an embedded channel write/erase flash memory cell as claimed in claim 9, wherein said electrical short circuit is formed by using a metal contact to connect said exposed n-type region in said deep p-type region with said deep p-type region.

[c12] 12.The structure of an embedded channel write/erase flash memory cell as claimed in claim 9, wherein said n-type semiconductors and said p-type semiconductors can be interchanged with each other, e.g., an npn structure can be replaced with a pnp structure.

[c13] 13.The structure of an embedded channel write/erase flash memory cell as

claimed in claim 1, wherein said CMOS device region further comprises a first P-well formed on in said substrate and at one side of said first deep P-well.

[c14] 14.The structure of an embedded channel write/erase flash memory cell as claimed in claim 13, wherein said CMOS device region further comprises a second P-well formed on said substrate and at one said of said first P-well.

[c15] 15.The structure of an embedded channel write/erase flash memory cell as claimed in claim 1, wherein said CMOS device region further comprises a first P-well formed on in said first deep P-well.

[c16] 16.The structure of an embedded channel write/erase flash memory cell as claimed in claim 1, wherein said CMOS device region further comprises a second P-well formed on in said second deep P-well.